MOTOROLA

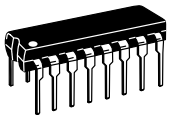
MC74AC190

Up/Down Counter with Preset and Ripple Clock

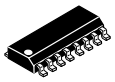
UP/DOWN COUNTER WITH PRESET AND RIPPLE CLOCK

The MC74AC190 is a reversible BCD (8421) decade counter which features synchronous counting and asynchronous presetting. The preset feature allows the MC74AC190 to be used in programmable dividers. The Count Enable input, the Terminal Count output and the Ripple Clock output make possible a variety of methods of implementing multistage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

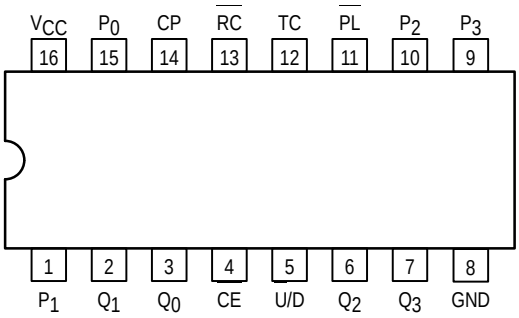
- High-Speed — 120 MHz Typical Count Frequency
- Synchronous Counting
- Asynchronous Parallel Load
- Cascadable
- Outputs Source/Sink 24 mA



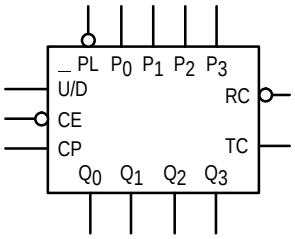
N SUFFIX
CASE 648-08
PLASTIC



D SUFFIX
CASE 751B-05
PLASTIC



LOGIC SYMBOL



PIN NAMES

$\overline{CE}$	Count Enable Input
CP	Clock Pulse Input
P_0–P_3	Parallel Data Inputs
$\overline{PL}$	Asynchronous Parallel Load Input
U/D	Up/Down Count Control Input
Q_0–Q_3	Flip-Flop Outputs
RC	Ripple Clock Output
TC	Terminal Count Output

FUNCTIONAL DESCRIPTION

The MC74AC190 is a synchronous up/down BCD decade counter. It contains four edge-triggered flip-flops with internal gating and steering logic to provide individual preset, count-up and count-down operations.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset to any desired number. When the Parallel Load (PL) input is LOW, information present on the Parallel Load inputs (P_0–P_3) is loaded into the counter and appears on the Q outputs. This operation overrides the counting functions, as indicated in the Mode Select Table.

A HIGH signal on the CE input inhibits counting. When CE is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The direction of counting is determined by the U/D input signal, as indicated in the Mode Select Table. CE and U/D can be changed with the clock in either state, provided only that the recommended setup and hold times are observed.

Two types of outputs are provided as overflow/underflow indicators. The terminal count (TC) output is normally LOW. It goes HIGH when the circuits reach zero in the count down mode or 9 in the count up mode. The TC output will then remain HIGH until a state change occurs, whether by counting or presetting or until U/D is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes.

The TC signal is also used internally to enable the Ripple Clock (RC) output. The RC output is normally HIGH. When CE is LOW and TC is HIGH, RC output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again. This feature simplifies the design of multistage counters, as indicated in Figures a and b. In Figure a, each RC output is used as the clock input for the next higher stage. This configuration is particularly advantageous when the clock source has a limited drive capability, since it drives only the first stage. To prevent counting in all stages it is only necessary to inhibit the first stage, since a HIGH signal on CE inhibits the RC output pulse, as indicated in the RC Truth Table. A disadvantage of this configuration, in some applications, is the timing skew between state changes in the first and lost stages. This represents the cumulative delay of the clock as it ripples through the preceding stages.

A method of causing state changes to occur simultaneously in all stages is shown in Figure b. All clock inputs are driven in parallel and the RC outputs propagate the carry/borrow signals in ripple fashion. In this configuration the LOW state duration of the clock must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. There is no such restriction on the HIGH state duration of the clock, since the RC output of any device goes HIGH shortly after its CP input goes HIGH.

The configuration shown in Figure c avoids ripple delays and their associated restrictions. The CE input for a given stage is formed by combining the TC signals from all the preceding stages. Note that in order to inhibit counting an enable signal must be included in each carry gate. The simple inhibit scheme of Figures a and b doesn't apply, because the TC output of a given stage is not affected by its own CE.

MODE SELECT TABLE

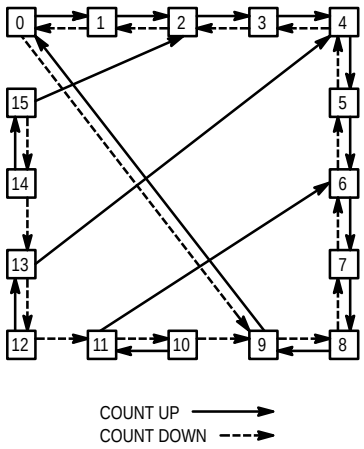
Inputs				Mode
$\overline{PL}$	$\overline{CE}$	$\overline{U/D}$	CP	
H	L	L	⌐‾|	Count Up
H	L	H	⌐‾|	Count Down
L	X	X	X	Preset (Asyn.)
H	H	X	X	No Change (Hold)

$\overline{RC}$ TRUTH TABLE

Inputs				Output
$\overline{PL}$	$\overline{CE}$	TC*	CP	$\overline{RC}$
H	L	H	⌐‾|	⌐‾|
H	H	X	X	H
H	X	L	X	H
L	X	X	X	H

*TC is generated internally
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐‾| = LOW-to-HIGH Transition

STATE DIAGRAM



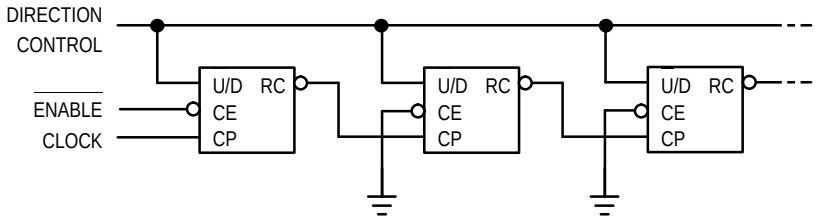


Figure a: N-Stage Counter Using Ripple Clock

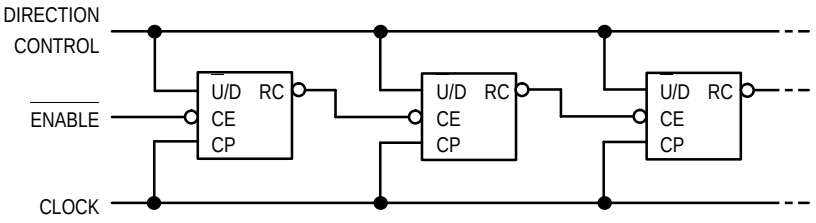


Figure b: Synchronous N-Stage Counter Using Ripple Carry/Borrow

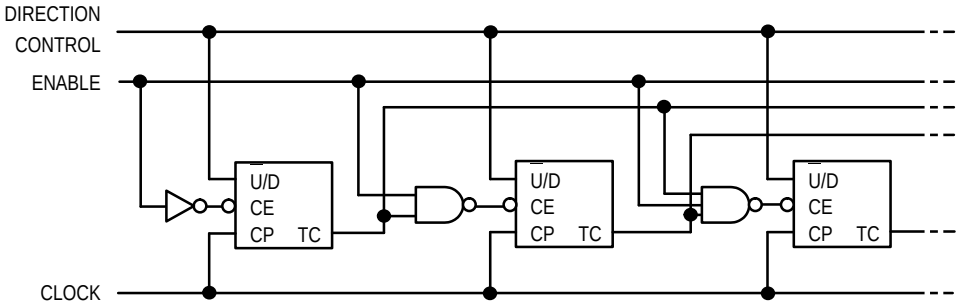
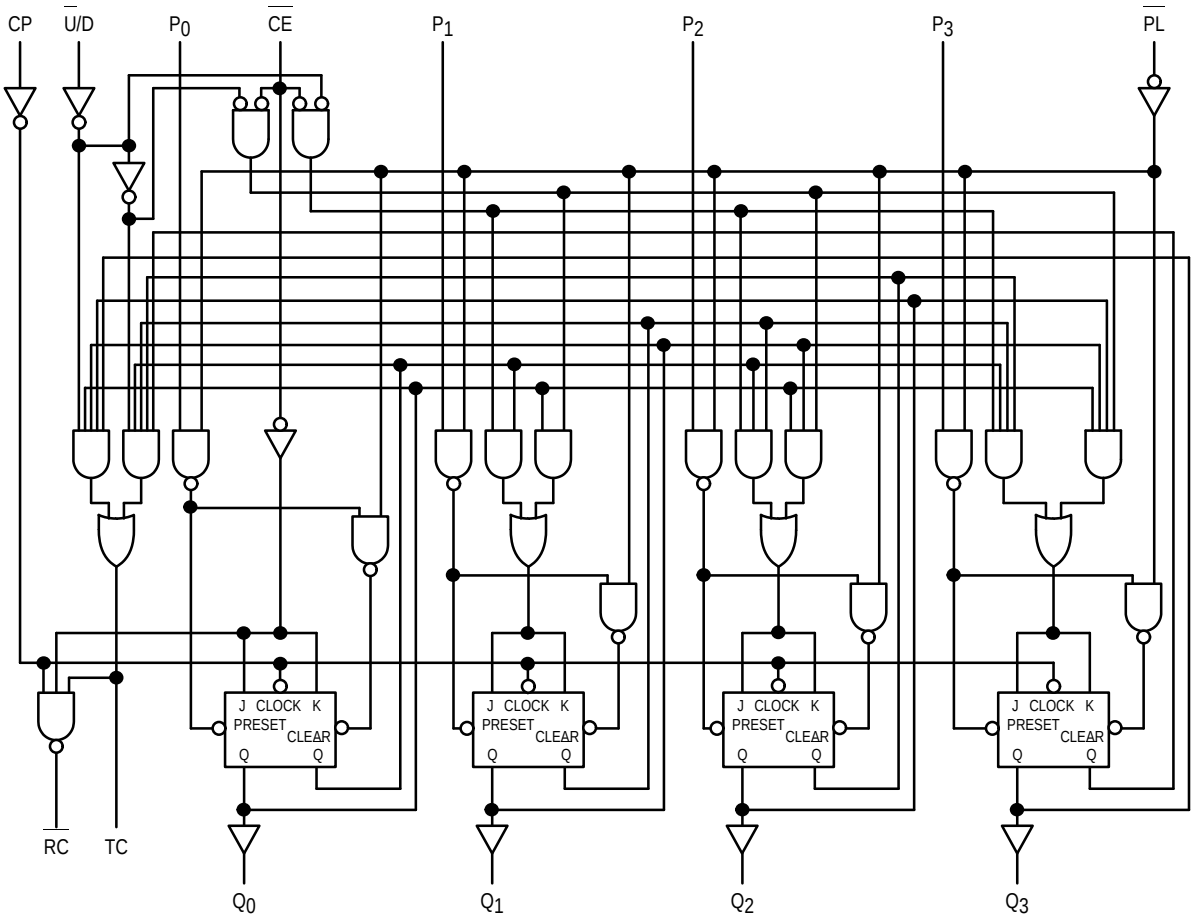


Figure c: Synchronous N-Stage Counter With Parallel Gated Carry/Borrow

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	–0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	–0.5 to V_{CC} +0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	–0.5 to V_{CC} +0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Sink/Source Current, per Pin	±50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	±50	mA
T_{stg}	Storage Temperature	–65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	′AC	2.0	5.0	6.0	V
		′ACT	4.5	5.0	5.5	
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Ref. to GND)		0		V_{CC}	V
t_r, t_f	Input Rise and Fall Time (Note 1) ′AC Devices except Schmitt Inputs	V_{CC} @ 3.0 V		150		ns/V
		V_{CC} @ 4.5 V		40		
		V_{CC} @ 5.5 V		25		
t_r, t_f	Input Rise and Fall Time (Note 2) ′ACT Devices except Schmitt Inputs	V_{CC} @ 4.5 V		10		ns/V
		V_{CC} @ 5.5 V		8.0		
T_J	Junction Temperature (PDIP)				140	°C
T_A	Operating Ambient Temperature Range		–40	25	85	°C
I_{OH}	Output Current — High				–24	mA
I_{OL}	Output Current — Low				24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		74AC T_A = –40°C to +85°C	Unit	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V_{OUT} = 0.1 V or V_{CC} – 0.1 V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V_{OUT} = 0.1 V or V_{CC} – 0.1 V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = –50 μA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0		2.56	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} –12 mA
		4.5		3.86	3.76		I_{OH} –24 mA
		5.5		4.86	4.76		–24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0		0.36	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.44		I_{OL} 24 mA
		5.5		0.36	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V_I = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V_{OLD} = 1.65 V Max
I_{OHD}		5.5			–75	mA	V_{OHD} = 3.85 V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V_{IN} = V_{CC} or GND

* All outputs loaded; thresholds on input associated with output under test.
† Maximum test duration 2.0 ms, one output loaded at a time.
Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC190 T_A = +25°C C_L = 50 pF			74AC190 T_A = –40°C to +85°C C_L = 50 pF		Unit	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Count Frequency	3.3 5.0	80 110					MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n	3.3 5.0	2.0 1.5		1.4 9.5	2.0 2.0	15.5 11.0	ns	3-6
t_{PHL}	Propagation Delay CP to Q_n	3.3 5.0	2.5 1.5		14.5 10.0	2.0 2.0	16.0 11.5	ns	3-6
t_{PLH}	Propagation Delay CP to TC	3.3 5.0	3.5 2.5		17.0 11.5	2.0 2.0	18.5 13.0	ns	3-6
t_{PHL}	Propagation Delay CP to TC	3.3 5.0	3.5 2.5		17.0 12.5	2.0 2.0	18.5 13.0	ns	3-6
t_{PLH}	Propagation Delay CP to RC	3.3 5.0	2.5 2.0		11.5 7.5	2.0 2.0	13.0 9.5	ns	3-6
t_{PHL}	Propagation Delay CP to RC	3.3 5.0	2.5 1.5		11.0 8.0	2.0 2.0	12.5 9.5	ns	3-6
t_{PLH}	Propagation Delay CE to RC	3.3 5.0	2.5 1.5		12.0 8.0	2.0 2.0	13.0 9.0	ns	3-6
t_{PHL}	Propagation Delay CE to RC	3.3 5.0	2.0 1.5		13.0 8.0	2.0 2.0	14.5 9.0	ns	3-6
t_{PLH}	Propagation Delay U/D to RC	3.3 5.0	2.5 1.5		14.0 8.5	2.0 2.0	15.5 10.0	ns	3-6
t_{PHL}	Propagation Delay U/D to RC	3.3 5.0	2.5 2.5		13.0 8.5	2.0 2.0	14.5 10.0	ns	3-6
t_{PLH}	Propagation Delay U/D to TC	3.3 5.0	3.0 3.0		12.0 8.0	2.0 2.0	13.0 9.0	ns	3-6
t_{PHL}	Propagation Delay U/D to TC	3.3 5.0	3.0 3.0		12.0 8.0	2.0 2.0	13.0 9.0	ns	3-6
t_{PLH}	Propagation Delay P_n to Q_n	3.3 5.5	2.0 2.0		15.0 10.0	1.5 1.5	17.0 11.5	ns	3-6
t_{PHL}	Propagation Delay P_n to Q_n	3.3 5.0	2.0 2.0		14.0 9.5	1.5 1.5	16.0 11.0	ns	3-6
t_{PLH}	Propagation Delay PL to Q_n	3.3 5.0	3.0 3.0		18.0 10.5	2.0 2.0	19.5 12.5	ns	3-6
t_{PHL}	Propagation Delay PL to Q_n	3.3 5.0	2.5 2.0		15.0 10.5	2.0 2.0	17.0 12.0	ns	3-6

* Voltage Range 3.3 V is 3.3 V ±0.3 V.
Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC190 T_A = +25°C C_L = 50 pF		74AC190 T_A = –40°C to +85°C C_L = 50 pF	Unit	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW P_n to PL	3.3 5.0		0.5 0	0.5 0	ns	3-9
t_h	Hold Time, HIGH or LOW P_n to PL	3.3 5.0		0 0	0 0	ns	3-9
t_s	Setup Time, LOW CE to CP	3.3 5.0		6.5 4.5	7.5 5.0	ns	3-9
t_h	Hold Time, LOW CE to CP	3.3 5.0		0 0	0 0	ns	3-9
t_s	Setup Time, HIGH or LOW U/D to CP	3.3 5.0		8.5 5.0	9.5 6.0	ns	3-9
t_h	Hold Time HIGH or LOW U/D to CP	3.3 5.0		0 0	0 0	ns	3-9
t_w	PL Pulse Width, LOW	3.3 5.0		5.0 3.5	5.5 4.0	ns	3-6
t_w	CP Pulse Width, LOW	3.3 5.0		5.0 3.5	5.5 4.0	ns	3-6
t_{rec}	Recovery Time PL to CP	3.3 5.0		0.5 0	0.5 0	ns	3-9

* Voltage Range 3.3 V is 3.3 V ±0.3 V.
Voltage Range 5.0 V is 5.0 V ±0.5 V.

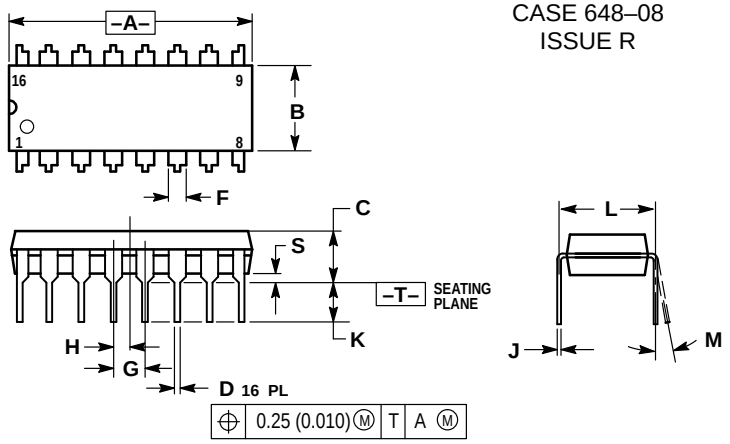
CAPACITANCE

Symbol	Parameter	Value Typ	Unit	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	75	pF	V_{CC} = 5.0 V

MC74AC190

OUTLINE DIMENSIONS

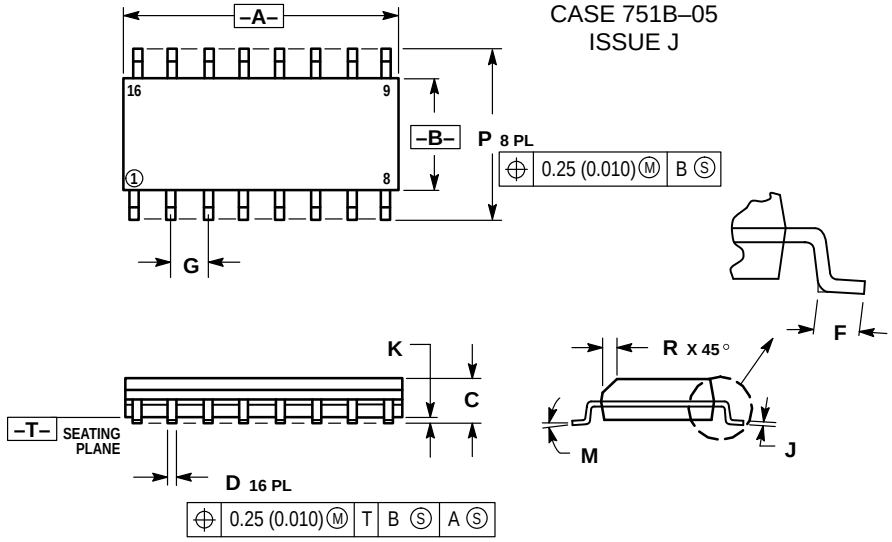
N SUFFIX
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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